~~13~~ 11.(Twice Amended) [A transistor comprising:

a source region;

a drain region;

a channel region between the source region and the drain region; and

a floating gate separated from the channel region by an insulator,] The transistor of claim 28 wherein a barrier energy between the floating gate and the insulator is less than approximately 3.3 eV.

~~14~~ 14.(Amended) The transistor of claim [11] ~~12~~ 11 28, wherein the floating gate is isolated from conductors and semiconductors.

~~15~~ 15.(Amended) The transistor of claim [11] ~~12~~ 11 28, wherein the insulator comprises a material that has a material composition that is selected to obtain a larger electron affinity than silicon dioxide.

~~16~~ 16.(Amended) The transistor of claim [11] 12 28, wherein the floating gate includes a material that has a material composition that is selected to obtain a smaller electron affinity than polycrystalline silicon.

~~17~~ 18.(Twice Amended) The transistor of claim [17] 12 28, wherein the area of a capacitor formed by the control electrode, the floating gate and the intergate dielectric is larger than the area of a capacitor formed by the floating gate, the insulator, and the channel region.

~~18~~ 17. ~~20~~ 20.(Amended) The transistor of claim [11] ~~18~~ 11 28, wherein the floating gate is capacitively separated from the channel region for providing transconductance gain.

Please add the following new claims:

~~33~~.(New) The memory device of claim ~~32~~ wherein a barrier energy between the floating gate and the insulator in each transistor is less than approximately 3.3 eV.

~~34~~.(New) The memory device of claim ~~33~~ wherein materials comprising at least one of the floating gate and the insulator in each transistor are selected to have an electron affinity causing the barrier energy to be less than approximately 3.3 eV.

~~35~~.(New) The memory device of claim ~~34~~ wherein the barrier energy is selected to obtain a data charge retention time for each transistor that is adapted for dynamic refreshing of charge stored on the floating gate.

~~36~~.(New) The memory device of claim ~~33~~ wherein the floating gate of each transistor is isolated from conductors and semiconductors.

~~37~~.(New) The memory device of claim ~~33~~ wherein the insulator in each transistor comprises a material that has a larger electron affinity than silicon dioxide.

~~38~~.(New) The memory device of claim ~~33~~ wherein the floating gate of each transistor comprises a material that has a smaller electron affinity than polycrystalline silicon.

~~39~~.(New) The memory device of claim ~~32~~ wherein the area of a capacitor formed by the control gate, the floating gate, and the intergate dielectric is larger than the area of a capacitor formed by the floating gate, the insulator, and the channel region of each transistor.

~~40~~.(New) The memory device of claim ~~32~~ wherein the floating gate of each transistor is capacitively separated from the channel region for providing transconductance gain.